EV077335368 #10-16-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/420,635
Filing Date ..... October 21, 1999
Inventor ..... Werner Juengling
Assignee ..... Micron Technology, Inc.
Group Art Unit 2812
Examiner ..... H. Tsai
Attorney's Docket No. MI22-1243
Title: Semiconductor Processing Methods of Forming Devices on a Substrate, Forming Device Arrays on a Substrate, Forming Conductive Lines on a Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated Circuitry

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Reference - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the reference listed on the attached Form PTO-1449. No admission is made regarding whether the submitted reference is prior art.

Citation of this reference is respectfully requested.

Respectfully submitted,

Date: Sept. 16, 2002

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